REMARKS

Claims 1 through 9 and 11 through 39 are pending in the application. The drawings were objected to under 37 C.F.R. § 1.83(a). In particular, the drawings were objected to as not showing a feature of the claims, namely "an importance level of the line after the valid data is accessed while maintaining the line as a valid line." Claim 30 is amended to correct a minor clerical error.

The drawings are amended, and are presently in condition to overcome previous objections. As indicated in Fig. 3, using the presently claimed invention provides changing the relative importance level for these cache lines while maintaining valid data in them. The support in the application as filed for the amendment to the drawings is described below. In view of the amendment to the drawings, reconsideration and withdrawal of the objections is respectfully requested.

Rejections of the Claims under 35 U.S.C. § 112, First Paragraph

Claims 1-39 were rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the enablement requirement. In regards to the Office Action's claim that the specification is silent on the use of indicating that the cache lines are valid, such is clearly shown in the specification (e.g., page 6, line 26 to page 7, line 14) and the drawings (e.g., Fig. 3). As presented in previous responses, the cited art describes invalidating cache lines, while in embodiments of the present invention, a cache line remains valid, but its importance level has been changed.

In regards to the clarification requested by the Office Action of the statement appearing on page 9, paragraph 2 of the response filed March 15, 2005, the confusion was due to a clerical error and should be disregarded. An explanation of the indicating the utility of RICL instruction is present immediately below.

Figure 3 describes an embodiment of the RICL instruction. In the third column of Fig. 3, the data for memory location b is loaded into cache line 1. This is shown diagrammatically in Fig. 3 in the second row (row Q) where the Allocation is reflected as "b==>1." As seen from Fig. 3, cache line 1 becomes the most recently used cache line and is moved to the highest level of importance, row U. In the column preceding column 37, the CPU accesses the data from

memory location b from cache line 1. This is valid cache data, and cache line 1 is moved to the most recently used importance level (row U). The RICL instruction (as indicated by the arrow in Fig. 3) changes the importance level of cache line 1 to least recently used (row R). The contents of the cache lines 0-3 are the same for column 37 and the two columns preceding it. Thus, cache line 1 included valid data in the column preceding column 37 and includes valid data in column 37 as well. Since its importance level has been reduced, cache line 1 is selected for replacement and in column 39, the data from memory location b is replaced with data from memory location e.

Therefore, using the RICL instruction to reduce the importance level of cache line 1, allows other cache lines that would otherwise be at the lowest importance level to be available for future accesses. Now compare this with the results of implementing the same access sequence without the RICL instruction. For example, take the data from memory location a in the column preceding column 37. Now assume after b is loaded, we proceed as if the RICL instruction is *not* implemented, and jump to the instruction found in column 38 (loading of e). Without the RICL instruction, data from memory location a stored in cache line 0 would have been replaced with data from memory location e. In the column immediately after column 38, the access to data from memory location a would result in a "cache miss" and the resulting delays associated with it.

Accordingly, reconsideration and withdrawal of the rejection of claims 1-39 under 35 U.S.C. § 112, first paragraph is respectfully requested.

In view of the above remarks, the Applicant respectfully submits that the present case is in condition for allowance and respectfully requests that the Examiner issue a notice of allowance for all currently pending claims.

The Office is hereby authorized to charge any fees determined to be necessary under 37 C.F.R. § 1.16 or § 1.17 or credit any overpayment to Kenyon & Kenyon **Deposit Account No. 11-0600**.

The Examiner is invited to contact the undersigned at (408) 975-7950 to discuss any matter concerning this application.

Respectfully submitted,

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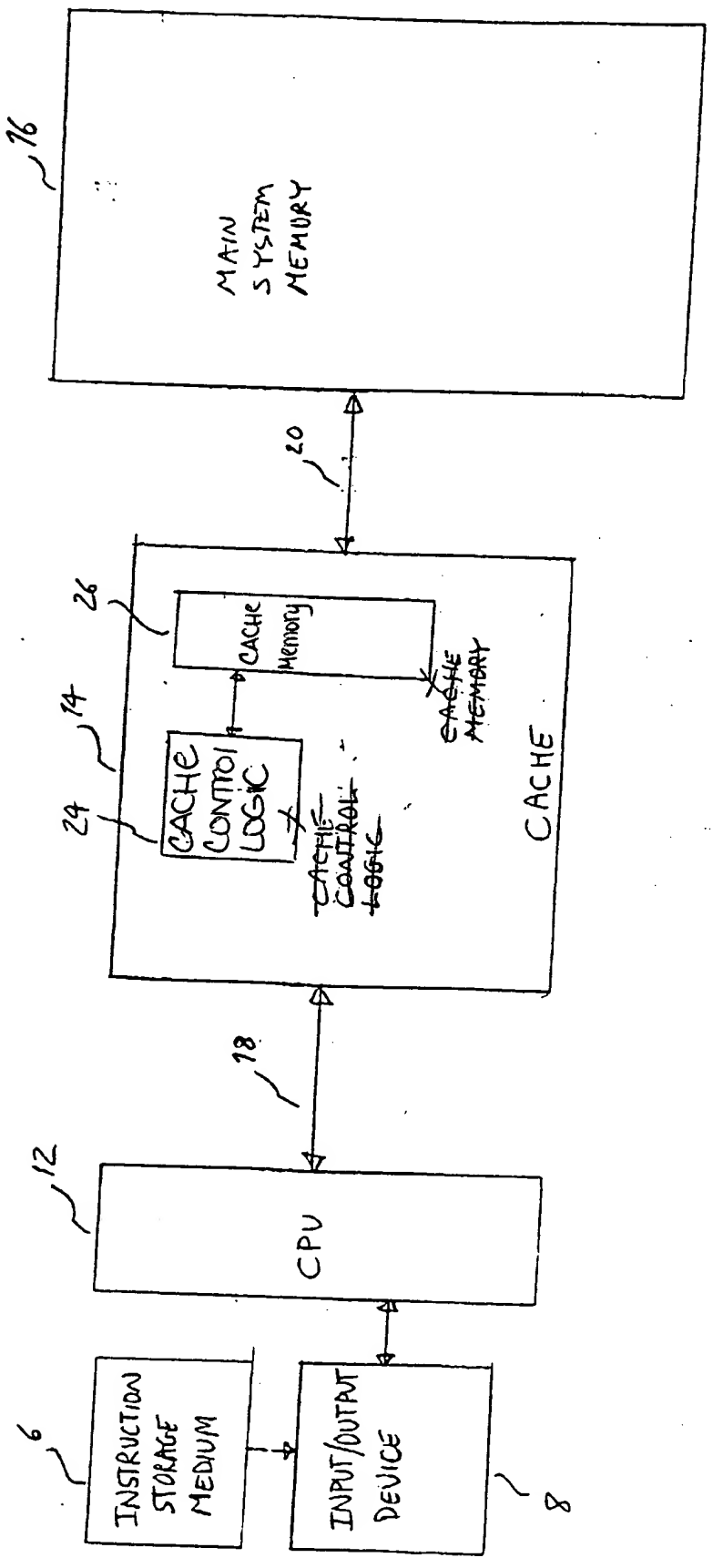

Figure 1
~~FIG. 1~~

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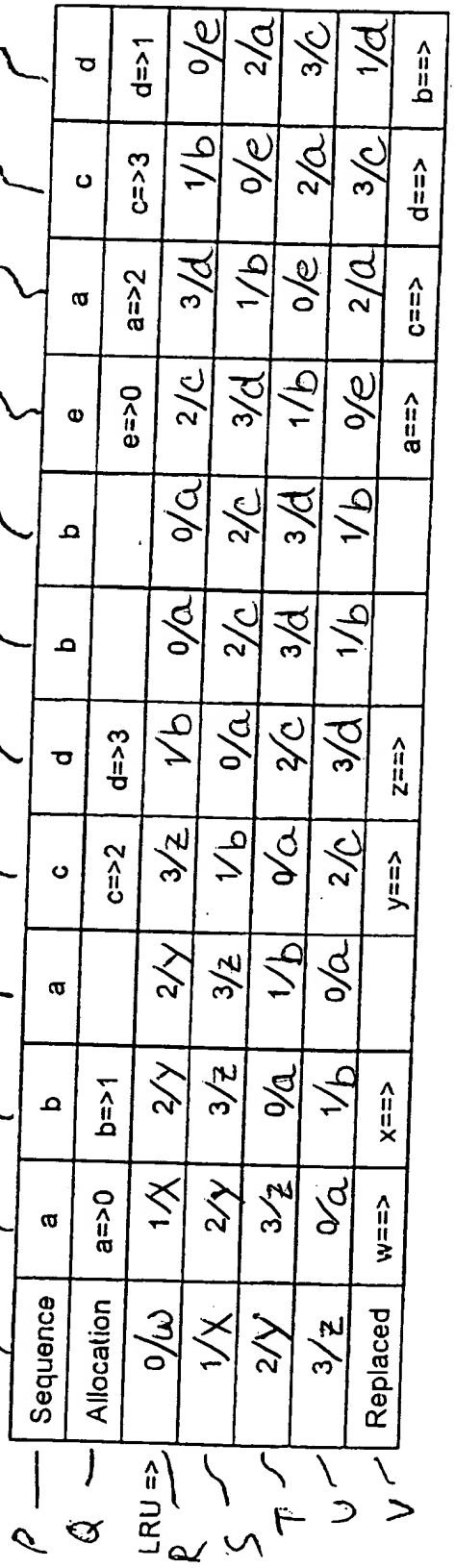

PRIOR ART

Fig. 2

Figure 2
(Prior Art)

Annotated Sheet 2 of 3
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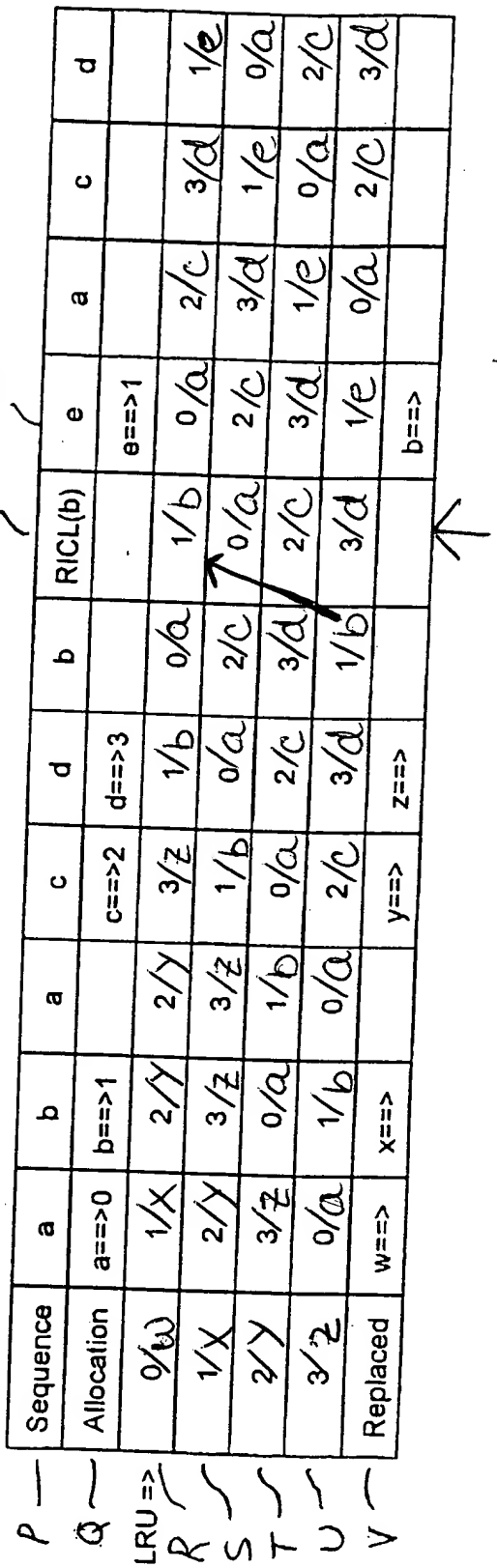

Importance level of cache line is reduced; cache line b continues to store valid data

~~Fig. 3~~

Figure 3